What is claimed is:

1. Apparatus for converting serial data clocked in response to a first clock signal having cycles occurring at a first rate to serial data clocked in response to a second clock signal having cycles occurring at a second rate, the second rate being equal to or greater than the first rate, the apparatus comprising:

first flip-flops arranged to store the data clocked in response to the first clock signal; a first signal generator responsive to the first clock signal arranged to generate a first enable signal after a predetermined number of cycles of the first clock signal dependant on the number of first flip-flops;

second flip-flops responsive to the first enable signal and the first clock signal arranged to store the data;

a second signal generator arranged to generate a second enable signal in response to the second clock signal and the first enable signal;

third flip-flops arranged to store the data in response to the second enable signal and the second clock signal; and

a multiplexer arranged to transmit the data in serial form from the third flip-flops at the second rate.

2. The apparatus of claim 1 wherein the first flip-flops comprise a serial chain of flip-flops arranged so that the data is stored in the first flip-flops in response to a plurality of cycles of the first clock signal.

3. The apparatus of claim 1 wherein the second flip-flops are arranged so that the data is stored in the second flip-flops in response to a single cycle of the first clock signal.

4. The apparatus of claim 1 wherein the third flip-flops are arranged so that the data is stored in the third flip-flops in response to a single cycle of the second clock signal.

5. The apparatus of claim 1 wherein the first signal generator comprises a counter and a comparator

arranged to generate the first enable signal in response to the predetermined number of cycles.

6. The apparatus of claim 1 wherein the second signal generator comprises flip-flops arranged to count a predetermined number of cycles of the second clock signal before generating the second enable signal.

7. The apparatus of claim 1 wherein the multiplexer enables transmission of data from the third flip-flops one-time-at-a-time in succession.

8. The apparatus of claim 1 wherein the number of first flip-flops is three or less.

9. A method of converting serial data clocked in response to a first clock signal having cycles occurring at the first rate to serial data clocked in response to a second clock signal having cycles occurring at a second rate, the second rate being equal to or greater than the first rate, the method comprising:

storing the data clocked in response to the first clock signal;

generating a first enable signal after a predetermined number of cycles of the first clock signal dependant on the number of bits of the data stored;

storing the data in response to the first enable signal and the first clock signal;

generating a second enable signal in response to the second clock signal and the first enable signal;

storing the data in response to the second enable signal and the second clock signal; and

transmitting the data in serial form at the second rate in response to the second clock signal.

10. The method of claim 9 wherein said storing the data clocked in response to the first clock signal comprises storing the data in response to a plurality of cycles of the first clock signal.

11. The method of claim 9 wherein said storing the data in response to the first enable signal and the first clock signal comprises storing in the data in response to a single cycle of the first clock signal.

12. The method of claim 9 wherein said storing the data in response to the second enable signal and the

second clock signal comprises storing the data in response to a single cycle of the second clock signal.

13. The method of claim 9 wherein said generating a first enable signal comprises:

counting cycles of the first clock signal to generate a sum signal; and

comparing the sum signal with the predetermined number of cycles.

14. The method of claim 9 wherein said generating a second enable signal comprises counting a predetermined number of cycles of the second clock signal before generating the second enable signal.

15. The method of claim 9 wherein said transmitting comprises transmitting the data stored in response to the second enable signal and the second clock signal one-bit-at-a-time in succession.

16. The apparatus of claim 9 wherein the number of bits of the data stored in response to the first clock signal comprises three bits or less.

17. The method of claim 9 wherein said storing the data clocked in response to the first clock signal comprises storing the data serially.

18. The method of claim 9 wherein said storing the data in response to the first enable signal and the first clock signal comprises storing the data in parallel.

19. In a data communication system comprising a plurality of channels receiving serial input data clocked in response to a plurality of first clock signals having cycles occurring at a plurality of different first rates, apparatus for converting serial input data to serial data clocked in response to a second clock signal having cycles occurring at a second rate, the second rate being equal to or greater than each of the first rates, the apparatus comprising:

a plurality of groups of first flip-flops arranged to store the input data clocked in response to the first clock signals, each group of first flip-flops corresponding to one of the channels;

a first signal generator responsive to the first clock signals to generate first enable signals, each first enable signal corresponding to one group the first flip-flops;

a plurality of groups of second flip-flops responsive to the first enable signals and the first clock signals to store the input data, each group of second flip-flops corresponding to one group of the first flip-flops;

a second signal generator responsive to the second clock signal and at least one of first enable signals to generate a second enable signal;

a plurality of groups of third flip-flops responsive to the second enable signal and the second clock signal to store the input data, each group of third flip-flops corresponding to one group of second flip-flops; and

a multiplexer arranged to transmit the input data in serial form from the third flip-flops at the second rate.

20. The apparatus of claim 19 wherein the first flip-flops comprise a serial chain of flip-flops arranged so that the data is stored in the first flip-flops in response to a plurality of cycles of the first clock signals.

21. The apparatus of claim 19 wherein the second flip-flops are arranged so that the data is stored in the second flip-flops in response to a single cycle of the first clock signals.

22. The apparatus of claim 19 wherein the third flip-flops are arranged so that the data is stored in the third flip-flops in response to a single cycle of the second clock signal.

23. The apparatus of claim 19 wherein the first signal generator comprises counters and comparators arranged to generate each of the first enable signals in response to a predetermined number of cycles of the one of the first clock signals.

24. The apparatus of claim 19 wherein the second signal generator comprises flip-flops arranged to count

a predetermined number of cycles of the second clock signal before generating the second enable signal.

25. The apparatus of claim 19 wherein the multiplexer enables transmission of data from the third flip-flops one-time-at-a-time in succession.

26. The apparatus of claim 19 wherein the number of first flip-flops is three or less per group.

27. In a data communication system comprising a plurality of channels receiving serial input data clocked in response to a plurality of first clock signals having cycles occurring at a plurality of different first rates, a method of converting serial input data to serial data clocked in response to a second clock signal having cycles occurring at a second rate, the second rate being equal to or greater than each of the first rates, the method comprising:

storing the input data clocked in response to the first clock signals separately for each channel;

generating first enable signals in response to the first clock signals, each first enable signal corresponding to one of the channels;

storing the input data in response to the first enable signals and the first clock signals separately for each channel;

generating a second enable signal in response to the second clock signal and at least one of first enable signals;

storing the input data in response to the second enable signal and the second clock signal separately for each channel; and

transmitting the stored input data in serial form at the second rate.

28. The method of claim 27 wherein said storing the input data clocked in response to the first clock signals separately for each channel comprises storing the input data in response to a plurality of cycles of the first clock signals.

29. The method of claim 27 wherein said storing the input data in response to the first enable signals and the first clock signals separately for each channel comprises storing the input data in response to a single cycle of the first clock signals.

30. The method of claim 27 wherein said storing the input data in response to the second enable signal and the second clock signal separately for each channel comprises storing the input data in response to a single cycle of the second clock signal.

31. The method of claim 27 wherein said generating the first enable signals comprises counting cycles of the first clock signals and generating each of the first enable signals in response to a predetermined number of cycles of the one of the first clock signals.

32. The method of claim 27 wherein said generating the second enable signal comprises counting a predetermined number of cycles of the second clock signal before generating the second enable signal.

33. The method of claim 27 wherein said transmitting comprises transmitting bits of the stored data one-bit-at-a-time in succession.

34. The method of claim 27 wherein the number of bits of the input data stored in response to the first clock signals per channel is three bits or less.

35. The method of claim 27 wherein said storing the input data clocked in response to the first clock signals comprises storing the data serially.

36. The method of claim 27 wherein said storing the input data in response to the first enable signals and the first clock signals comprises storing the data in parallel.